## Estimating Power for ADSP-TS201S TigerSHARC® Processors

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## Introduction

This EE-Note discusses techniques for estimating the power consumption for an ADSP-TS201S TigerSHARC® processor. This document assists board designers by providing data and recommendations, allowing them to estimate their budgets for power supply and thermal relief designs for a given system.

ADSP-TS201S processors are members of the ultra-high-performance, static superscalar, 32-bit TigerSHARC processor family. This processor is offered in two different speed grades, which allow the core to operate at a maximum clock frequency of either 500 or 600 MHz. The processor also requires three separate external voltage supplies, as shown in Table 1.

| ADSP-TS201S Voltage Domain | Core Clock Rate 500 MHz | Core Clock Rate 600 MHz |
|---|---|---|
| $V_{DD}$ | 1.05V +/- 5% | 1.20V +/- 5% |
| $V_{DD\_DRAM}$ | 1.50V +/- 5% | 1.60V +/- 5% |
| $V_{DD\_IO}$ | 2.50V +/- 5% | 2.50V +/- 5% |

*Table 1. Voltage Supply Requirements*

## Power Consumption

The total power consumed by the ADSP-TS201S device is the sum of the power consumed on each of the voltage domains ($V_{DD}$, $V_{DD\_DRAM}$, $V_{DD\_IO}$) of the processor. This sum consists of the internal core logic, the I/O logic, the internal DRAM, and the related circuitry for each of these domains.

The following sections explain how to derive power numbers for a given system based on the different internal dynamic activity levels (instruction, data, and DMA sequence), I/O activity, and environmental operating conditions. Details describing the activity levels are also provided.

## $V_{DD}$ Current Consumption

The total internal current consumption ($I_{DD}$) on the $V_{DD}$ supply is the sum of the static and dynamic components of the processor.

Since the dynamic activity of the processor is dependent on the instruction execution sequence of the application code and the data operands involved, a good understanding of the instruction execution is important in estimating the dynamic current ($I_{DD\_DYN}$) consumed by the processor core. The dynamic current consumption can be calculated by multiplying the weighted average of the different activity levels by a baseline dynamic current characteristic. For details on this characteristic, see *IDD_BASELINE Dynamic Current Characteristic Graph*.

A precise understanding of the application program can be achieved by profiling the program execution (or by accurately estimating the average code activity levels for specific portions of the program). The goal of profiling is to determine the percentage of execution time each activity level occupies. These dynamic core activity levels are explained in detail in the following section.

## Internal Dynamic Activity Level Definitions

The following definitions apply to the internal dynamic activity levels ($I_{DD\_DYN}$) shown in Table 2. Excluding the $I_{DD\_DMA}$ and $I_{DD\_IDLE}$ activity levels, each activity level contains no stall cycles, and therefore represents worst-case processor core activity.

- **IDD_CLU_HIGH** – *S*ustained high-activity operations of the *CLU* defined as an *XCORRS* instruction along with two parallel quad-word data fetches executing every cycle. Concurrently, either a 64-bit parallel *ALU*, a *SIMD* quad 16-bit complex multiply, or a 64-bit dual-Trellis History register update operation is executed in the same cycle. The data fetched and operated on are random; the data and instructions reside in independent memory segments to allow the highest data throughput and to ensure that no stall cycles are incurred. This $I_{DD\_CLU\_HIGH}$ activity level also includes a concurrent external port DMA sequence, as described in the $I_{DD\_DMA}$ activity level.

- **IDD_CLU_TYP** – *S*ustained typical activity operations of the *CLU* defined as a combination of the *ACS* and *PERMUTE* instructions: The *ACS* instruction occurs in parallel with a quad-word Trellis History register read, along with a long-word memory access; the *PERMUTE* instruction occurs in parallel with two quad-word data fetches. The data fetched and operated on are random; the data and instructions reside in independent memory segments to allow the highest data throughput and to ensure that no stall cycles are incurred. This $I_{DD\_CLU\_TYP}$ activity level also includes a concurrent external port DMA sequence, as described in the $I_{DD\_DMA}$ activity level.

- **IDD_CLU_LOW** – *S*ustained low-activity operations of the *CLU* defined as either a *TMAX* or *MAX* instruction, along with two parallel quad-word data fetches, and a shifter operation occurring in each compute block executing every cycle. The data fetched and operated on are random; the data and instructions reside in independent memory segments to allow the highest data throughput and to ensure that no stall cycles are incurred. This $I_{DD\_CLU\_LOW}$ activity level also includes a concurrent external port DMA sequence, as described in the $I_{DD\_DMA}$ activity level.

- **IDD_FFT** – *S*ustained high-activity floating-point operations of the computational units of the processor core. This activity level is a *SIMD* floating-point add/subtract dual operation along with one of the following: a quad-word merged access, a single quad-word data access, a *SIMD* floating-point multiply, and a quad-word merged access; or a *SIMD* floating-point multiply, a quad-word merged access, and a long-word access to two general-purpose registers within one of the computational units. The data fetched and operated on are random; data and instructions reside in independent memory segments to allow the highest data throughput and to ensure that no stall cycles are incurred. This $I_{DD\_FFT}$ activity level also includes a concurrent external port DMA sequence, as described in the $I_{DD\_DMA}$ activity level.

- **IDD_COMPUTE_HIGH** – *S*ustained high-activity operations of the computational units of the processor core. This activity level is one of the following: a *SIMD* quad 16-bit fixed-point multiply and a *SIMD* quad 16-bit fixed-point addition in parallel, or a *SIMD* extended floating-point multiply and a *SIMD* extended floating-point addition in parallel. Concurrently, dual merged-memory fetches are executed. The data fetched and operated on are random. This $I_{DD\_COMPUTE\_HIGH}$ activity level definition also includes a concurrent external port DMA sequence, as described in the $I_{DD\_DMA}$ activity level definition below.

- **IDD_COMPUTE_TYP** – *S*ustained typical activity operations of the computational units of the processor core. This activity level is one of the following: a *SIMD* quad 16-bit fixed-point multiply, a *SIMD* quad 16-bit fixed-point addition, a *SIMD* extended-precision floating-point multiply, or a *SIMD* extended-precision floating-point addition. One of these instructions occurs in parallel with two quad-word data fetches. The data fetched and operated on are random. This $I_{DD\_COMPUTE\_TYP}$ activity level also includes a concurrent external port DMA sequence, as described in the $I_{DD\_DMA}$ activity level.

- **IDD_CTRL** – Control activity is a continuous decision-making sequence of instructions and predicted branches. The branch prediction is deliberately set to be incorrect 50% of the time to allow for equal distribution. This $I_{DD\_CTRL}$ activity level definition also includes the DMA activity level as described in the $I_{DD\_DMA}$ activity level.

- **IDD_DMA** – DMA activity is a single-channel external port DMA from external memory to internal memory, using quad-word transfers of 32 words total. The DMA is chained to itself (in order to run continuously), and does not use interrupts. After initializing the DMA sequence, the processor core is not involved; it executes the IDLE;; instruction only.

- **IDD_IDLE** – $V_{DD}$ supply current for idle activity. This activity level is defined as the processor core executing an IDLE;; instruction only, with no active DMAs or interrupts.

## Estimating Dynamic Current Consumption

Two steps are involved in estimating the dynamic current consumption on the $V_{DD}$ domain. The first step determines the dynamic baseline current. The second step determines the percentage of activity for each of the discrete vectors with respect to the entire application code.

### $I_{DD\_BASELINE}$ Dynamic Current Characteristic Graph

The ADSP-TS201S $I_{DD\_BASELINE}$ dynamic current characteristic graph is shown in Figure 1. (Appendix B contains a larger image of this graph.) Each line in the graph represents a baseline $I_{DD}$ dynamic internal current value for a specific given voltage. To calculate the baseline dynamic current ($I_{DD\_BASELINE}$) on the $V_{DD}$ voltage domain, take the line on the graph that represents the operating voltage of the processor and find the point on this line for the specific operating frequency of each processor in the system. From this point on the curve, the baseline value for the dynamic current can be determined by finding its point of intersection with the vertical axis on the left side labeled "Dynamic Current".
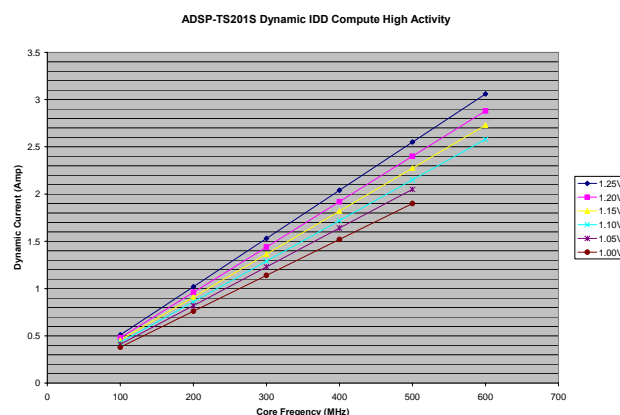


*Figure 1. Dynamic Baseline Current Characteristic*

Assume that the TigerSHARC processors in the example system are operating at 500 MHz at 1.05 V. From the graph in Figure 1, these two parameters will yield a result of 2.05 A for the dynamic baseline current.

From the activity level definitions described in *Internal Dynamic Activity Level Definitions*, and after profiling the application program, the percentage of overall execution time for each activity level can be determined.

Table 2 lists the scale factor for each activity level, which are used to estimate the dynamic current ($I_{DD\_DYN}$) for a specific application.

| Power Vector Name | Activity Factor Value |
|---|---|
| $I_{DD\_CLU\_HIGH}$ | 1.45 |
| $I_{DD\_CLU\_TYP}$ | 1.14 |
| $I_{DD\_CLU\_LOW}$ | 0.98 |
| $I_{DD\_FFT}$ | 1.17 |
| $I_{DD\_COMPUTE\_HIGH}$ | 1.00 |
| $I_{DD\_COMPUTE\_TYP}$ | 0.85 |
| $I_{DD\_CTRL}$ | 0.71 |
| $I_{DD\_DMA}$ | 0.57 |
| $I_{DD\_IDLE}$ | 0.55 |

Table 2. Internal Dynamic Core Current (IDD_DYN)

The processor core dynamic current can be calculated by multiplying the value of the dynamic baseline current by the activity factor value for each discrete vector, and then multiplying this result by the percentage of time spent for each vector in the application program. This step is shown in Equation 1.

$$(\% I_{DD\_CLU\_HIGH} \; x \; I_{DD\_CLU\_HIGH} \; Activity \; Factor \; x \; I_{DD\_BASELINE})$$
$$(\% I_{DD\_CLU\_TYP} \; x \; I_{DD\_CLU\_TYP} \; Activity \; Factor \; x \; I_{DD\_BASELINE})$$
$$(\% I_{DD\_CLU\_LOW} \; x \; I_{DD\_CLU\_LOW} \; Activity \; Factor \; x \; I_{DD\_BASELINE})$$
$$(\% I_{DD\_FFT} \; x \; I_{DD\_FFT} \; Activity \; Factor \; x \; I_{DD\_BASELINE})$$
$$(\% I_{DD\_COMPUTE\_HIGH} \; x \; I_{DD\_COMP\_HIGH} \; Activity \; Factor \; x \; I_{DD\_BASELINE})$$
$$(\% I_{DD\_COMPUTE\_TYP} \; x \; I_{DD\_COMP\_TYP} \; Activity \; Factor \; x \; I_{DD\_BASELINE})$$
$$(\% I_{DD\_CTRL} \; x \; I_{DD\_CTRL} \; Activity \; Factor \; x \; I_{DD\_BASELINE})$$
$$(\% I_{DD\_DMA} \; x \; I_{DD\_DMA} \; Activity \; Factor \; x \; I_{DD\_BASELINE})$$
$$+ (\% I_{DD\_IDLE} \; x \; I_{DD\_IDLE} \; Activity \; Factor \; x \; I_{DD\_BASELINE})$$
$$= Total \; Weighted \; Average \; Dynamic \; Current \; for \; V_{DD}$$
$$= I_{DD\_DYN}$$

Equation 1. $I_{DD\_DYN}$ Core Dynamic Current

Example: Assume that for a given system, the profile of the application code is as follows:

*0% IDD_CLU_HIGH Activity Level*
*0% IDD_CLU_TYP Activity Level*
*0% IDD_CLU_LOW Activity Level*
*15% IDD_FFT Activity Level*
*20% IDD_COMPUTE_ HIGH Activity Level*
*50% IDD_COMPUTE_ TYP Activity Level*
*15% IDD_CTRL Activity Level*
*0% IDD_DMA Activity Level*
*0% IDD_IDLE Activity Level*

*Example 1. Internal System Activity Level*

From the percentages of this example, the core dynamic current ($I_{DD\_DYN}$) for a single processor can be calculated using Equation 1 as follows:

$$(15\% \; x \; 1.17 \; x \; 2.05)$$
$$(20\% \; x \; 1.00 \; x \; 2.05)$$
$$(50\% \; x \; 0.85 \; x \; 2.05)$$
$$+ (15\% \; x \; 0.71 \; x \; 2.05)$$
$$= 1.86 \; A$$

*Example 2. Total Estimated Dynamic Current*

Therefore, the total estimated dynamic current on the $V_{DD}$ supply is 1.86 A.

## $I_{DD\_STATIC}$ Baseline Characteristic Curve

The $I_{DD\_STATIC}$ baseline characteristic curve is used to calculate the static power on the $V_{DD}$ voltage domain. Because the static power consumed on $V_{DD}$ is a function of temperature and voltage (and *not* a function of frequency), this static power level does not need to be calculated for each discrete internal power vector definition. The static power is simply added to the total estimated dynamic current value ($I_{DD\_DYN}$), which was calculated earlier.

Figure 2 shows the static baseline current for typical devices. A typical device is defined as a device whose static current consumption lies at the mid-point of the probability density distribution of the entire population of devices. The curves in Figure 2 can be used to calculate

the statistical average static power for all of the ADSP-TS201S devices in a system.
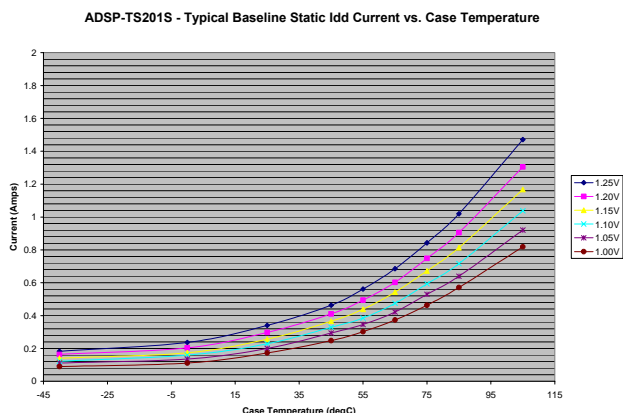


Figure 2. Typical Static Current Characteristic Graph

Each line in Figure 2 represents a baseline static internal current value at a given voltage. To calculate the total static current ($I_{DD\_STATIC}$) on the $V_{DD}$ voltage domain, take the line on the graph that represents the voltage of the device and find the point on this line for the specific case temperature at which the processors in the system will operate. From this point on the curve, the value for the baseline static current can be estimated by finding the point of intersection on the vertical axis on the left side of the graph labeled, "Static Current".

For the example system, assume that all of the processor cores operate at $V_{DD}$ = 1.05 V, and that due to system conditions, the maximum value for $T_{CASE}$ is 25°C. Therefore, from these operating conditions, Figure 2 shows that the static current consumed on the $V_{DD}$ voltage domain is 0.20 A.

### Total Estimated Core Current ($I_{DD}$)

To find the total $I_{DD}$ current consumption for each processor in a specific system, simply add the total dynamic and static current components on the $V_{DD}$ supply domain, as shown in Equation 2:

$$I_{DD} = I_{DD\_DYN} + I_{DD\_STATIC}$$

Equation 2. Total $I_{DD}$ Current

For the example system, calculate the total $I_{DD}$ current as follows:

$$I_{DD} = I_{DD\_DYN} + I_{DD\_STATIC}$$
$$= 1.86\ A + 0.20\ A$$
$$= 2.06\ A$$

Example 3. Total $I_{DD}$ Current Estimation

## $V_{DD\_A}$ Current Consumption

Each ADSP-TS201S processor includes an analog phase lock loop (PLL) and related circuitry to provide clock signals to the core and peripheral logic. This circuitry is powered from an external source that supplies power to the $V_{DD\_A}$ pins of the processor. Since this logic is always active, it must be considered when calculating the overall power consumed by each processor core.

There are two different speed grades (500 and 600 MHz) for the ADSP-TS201S processor, as well as two specific $V_{DD\_A}$ voltage requirements for each operating frequency. Therefore there are two different values for the typical and maximum $I_{DD\_A}$ current for each speed grade, respectively.

For 500 MHz speed grade devices, the typical current ($I_{DD\_A\ (TYP)}$) consumed by the analog circuitry of each processor is *20 mA*. The maximum $I_{DD\_A}$ current ($I_{DD\_A\ (MAX)}$) for each processor at 500 MHz is *50 mA*.

$$I_{DD\_A\ (TYP)} = 20\ mA$$

Equation 3. Typical 500 MHz $I_{DD\_A}$ Current

$$I_{DD\_A\ (MAX)} = 50\ mA$$

Equation 4. Maximum 500 MHz $I_{DD\_A}$ Current

For 600 MHz speed grade devices, the $I_{DD\_A}$ current increases slightly due to the increased operating voltage of the device. The typical current ($I_{DD\_A\ (TYP)}$) consumed by the analog circuitry of each processor is *25 mA*. The maximum $I_{DD\_A}$ current ($I_{DD\_A\ (MAX)}$) for each processor at 600 MHz is *55 mA*.

$$I_{DD\_A\ (TYP)} = 25\ mA$$

*Equation 5. Typical 600 MHz $I_{DD\_A}$ Current*

$$I_{DD\_A\ (MAX)} = 55\ mA$$

*Equation 6. Maximum 600 MHz $I_{DD\_A}$ Current*

## Total Estimated Internal Power ($P_{DD}$)

Since $V_{DD\_A}$ is derived from $V_{DD}$, the total estimated power ($P_{DD}$) consumed on the $V_{DD}$ voltage domain can be calculated as follows:

$$P_{DD} = V_{DD}\ x\ (I_{DD} + I_{DD\_A\ (TYP)})$$

*Equation 7. Total Internal Average Power Calculation*

For the example system, calculate $P_{DD}$ using Equation 7 to determine a total internal average power as shown in Example 4:

$$
\begin{aligned}
P_{DD} &= V_{DD}\ x\ (I_{DD} + I_{DD\_A\ (TYP)}) \\
&= 1.05\ V\ x\ (2.06\ A + 0.02\ A) \\
&= 2.18\ W
\end{aligned}
$$

*Example 4. Total Internal Average Power*

## $V_{DD\_DRAM}$ Current Consumption

The internal DRAM of the ADSP-TS201S processor *must* be supplied from an external voltage source.

The voltage requirement for the $V_{DD\_DRAM}$ supply is dependent upon the operating frequency of the processor. For 500 MHz speed grade devices, the $V_{DD\_DRAM}$ voltage domain requires a *1.50 V* supply. For 600 MHz devices, the internal DRAM should be supplied with *1.60 V*.

For a 500 MHz device, the typical current consumed by the internal DRAM ($I_{DD\_DRAM\ (TYP)}$) is *250 mA*. This value represents the current consumed during typical core and I/O activity using the internal DRAM. The typical power consumed by the internal DRAM ($P_{DD\_DRAM\ (TYP)}$) of the processor is *375 mW*.

$$I_{DD\_DRAM\ (TYP)} = 250\ mA$$

*Equation 8. Typical $I_{DD\_DRAM}$ Consumption (500 MHz)*

$$
\begin{aligned}
P_{DD\_DRAM\ (TYP)} &= V_{DD\_DRAM}\ x\ I_{DD\_DRAM\ (TYP)} \\
&= 1.5\ V\ x\ 250\ mA \\
&= 375\ mW
\end{aligned}
$$

*Example 5. Typical $P_{DD\_DRAM}$ Consumption (500 MHz)*

The total maximum current consumed by the internal DRAM of a 500 MHz device ($I_{DD\_DRAM\ (MAX)}$) is *400 mA*. Therefore, the total maximum power consumed by the internal DRAM ($P_{DD\_DRAM\ (MAX)}$) of the processor is *600 mW*.

$$I_{DD\_DRAM\ (MAX)} = 400\ mA$$

*Equation 9. Maximum $I_{DD\_DRAM}$ Consumption (500 MHz)*

$$
\begin{aligned}
P_{DD\_DRAM\ (MAX)} &= V_{DD\_DRAM}\ x\ I_{DD\_DRAM\ (MAX)} \\
&= 1.5\ V\ x\ 400\ mA \\
&= 600\ mW
\end{aligned}
$$

*Example 6. Maximum $P_{DD\_DRAM}$ Consumption (500 MHz)*

For a 600 MHz device, the typical current consumed by the internal DRAM ($I_{DD\_DRAM\ (TYP)}$) is *280 mA*. This value represents the current consumed during typical core and I/O activity using the internal DRAM. The typical power consumed by the internal DRAM ($P_{DD\_DRAM\ (TYP)}$) of the processor is *448 mW*.

$$I_{DD\_DRAM\ (TYP)} = 280\ mA$$

*Equation 10. Typical $I_{DD\_DRAM}$ Consumption (600 MHz)*

$$
\begin{aligned}
P_{DD\_DRAM\ (TYP)} &= V_{DD\_DRAM}\ x\ I_{DD\_DRAM\ (TYP)} \\
&= 1.6\ V\ x\ 280\ mA \\
&= 448\ mW
\end{aligned}
$$

*Example 7. Typical $P_{DD\_DRAM}$ Consumption (600 MHz)*

The total maximum current consumed by the internal DRAM of a 600 MHz device ($I_{DD\_DRAM\ (MAX)}$) is *430 mA*. Therefore, the total maximum

power consumed by the internal DRAM ($P_{DD\_DRAM\,(MAX)}$) of the processor is *688 mW*.

$$I_{DD\_DRAM\,(MAX)} = 430\ mA$$

*Equation 11. Maximum $I_{DD\_DRAM}$ Consumption (600 MHz)*

$$P_{DD\_DRAM\,(MAX)} = V_{DD\_DRAM}\ x\ I_{DD\_DRAM\,(MAX)}$$
$$= 1.6\ V\ x\ 430\ mA$$
$$= 688\ mW$$

*Example 8. Maximum $P_{DD\_DRAM}$ Consumption (600 MHz)*

# $V_{DD\_IO}$ Current Consumption

The total external power consumption ($P_{DD\_IO}$) on the $V_{DD\_IO}$ voltage domain is comprised of three components: the External Port, the Link Ports, and the associated circuitry for the external pins, output drivers, and control logic. Also, each of these three current components are comprised of static and dynamic sub-components.

## External Port Dynamic Current Estimation

The dynamic current consumption of the External Port on the $V_{DD\_IO}$ supply is caused by the switching of the output pins and is system dependent. For each unique group of pins, the magnitude of power consumed depends on:

1. The number of output pins that switch during each cycle, $O$
2. The load capacitance of the output pins, $C$
3. Their voltage swing, $V_{DD\_IO}$
4. The maximum frequency at which the pins can switch, $f$

The load capacitance should include the input capacitance of each connected device as well as the processor's own input capacitance ($C_{IN}$). For additional accuracy, trace capacitance should be included, if possible. The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum frequency of ½ SCLK.

Note that the total power measured on the $V_{DD\_IO}$ supply domain is calculated on a total system basis with regard to the dynamic External Port activity; it is not a cumulative result from the calculation of each processor in the system, since only one processor can be the bus master at any given time.

Equation 12 shows how to calculate the average dynamic current for the address, data, and control pins on the $V_{DD\_IO}$ supply that is consumed by the External Port, given the above four parameters:

$$I_{DD\_IO\_EP\_DYN} = O\ x\ C\ x\ V_{DD\_IO}\ x\ f$$

*Equation 12. External Port Average Dynamic Current*

Example: Calculate the average current consumed by the External Port pins on the $V_{DD\,IO}$ supply with the following assumptions:

- The example system consists of four ADSP-TS201S processors with one bank of shared external memory (64-bit), where $C_{IN}$ = 3 pF per TigerSHARC device.
- Two 1 M × 32-bit SDRAM chips are used, each with a load of 5 pF per pin (trace capacitance is neglected for this example).
- Continuous burst of quad-word (128-bit) writes occur every cycle at a rate of SCLK, with 50% of the data pins switching (this represents random data).
- The external address increments sequentially on a transaction boundary (every quad-word). For sequential addressing, the number of address bits switching approaches 2 bits.
- The control pins switch for refresh cycles and page boundary crossings.
- SCLK = 62.5 MHz (bus cycle time).

Using Equation 12, the average dynamic current ($I_{DD\_IO\_EP\_DYN}$) consumed by the External Port pins on the $V_{DD\_IO}$ supply is calculated for each class of pins that can drive as shown in Table 3.

| Pin Type | # of Pins | % Switching | x C | x V_{DD\_IO} | x f | = I_{DD\_IO\_EP\_DYN} |
|----------|-----------|-------------|-----|--------------|-----|----------------------|
| Data | 64 | 50 | 5 pF + 4 x C_{IN} | 2.5 V | 31.25 MHz | 0.0425 A |
| Addr | 32 | 6.25 | 10 pF + 4 x C_{IN} | 2.5 V | 15.625 MHz | 0.0017 A |
| Ctrl | 8 | 50 | 10 pF + 4 x C_{IN} | 2.5 V | 156.25 KHz | 0.0001 A |

Table 3. External Port Current Calculation Example

From the data in Table 3, the total average dynamic current consumed by the External Port of a single processor in the example system is calculated by summing the data from the right-most column of the table:

$$
\begin{array}{r}
0.0425\ A \\
0.0017\ A \\
+\ 0.0001\ A \\
\hline
I_{DD\_IO\_EP\_DYN}\ =0.0443\ A
\end{array}
$$

Example 9. External Port Total Average Dynamic Current Calculation

Note that the total average dynamic power measured on the $V_{DD\ IO}$ domain is calculated on a total system basis with regard to the External Port switching. For the External Port system example, the results given in Example 9 are for the entire External Port dynamic power consumption for the example four-processor system. In other words, this result is not added to the total current for each processor in the system, since only one processor can drive the cluster bus at any given time.

## External Port Static Current

One final component to discuss here is the static current consumed by the internal circuitry of the processor supplied by the $V_{DD\_IO}$ domain. The static current consumed by the External Port circuitry on the $V_{DD\_IO}$ domain is approximately 7.0 mA. Note that this 7 mA value is contributed by *each* processor in the system when calculating the overall current budget on the $V_{DD\_IO}$ domain.

$$I_{DD\_IO\_EP\_STATIC} = 7.0\ mA$$

Equation 13. External Port Static Current Consumption

## Total Estimated External Port Current ($I_{DD\_IO\_EP}$)

The total External Port current consumed by *each* processor on the cluster bus on the $V_{DD\_IO}$ domain is calculated as follows:

$$
\begin{array}{r}
I_{DD\_IO\_EP\_DYN}\ /\ N \\
+\quad I_{DD\_IO\_EP\_STATIC} \\
\hline
=\quad I_{DD\_IO\_EP}
\end{array}
$$

Where: N = the total number of ADSP-TS201S processors in the cluster

Equation 13. Total Estimated External Port Current per Processor

For the example system, the value of $I_{DD\_IO\_EP}$ for each processor can be estimated as shown in the following example:

$$
\begin{array}{r}
44.3\ mA\ /\ 4 \\
+\quad 7.0\ mA \\
\hline
=\quad 18.1\ mA
\end{array}
$$

Example 10. Total Estimated External Port Current Calculation per Processor

## Link Port Current Estimation

The Link Port current ($I_{DD\_IO\_LP}$) consumption on $V_{DD\_IO}$ domain is comprised of three different components: the external dynamic current, the internal static current, and the internal dynamic current.

The external dynamic current for a transmitting Link Port is negligible and can be ignored for the current consumption estimations. (This statement also holds true for a receiving Link Port.)

The output pins of the Link Ports are driven by current-mode drivers; thus the logic value of the differential output pins is determined by the *direction* of the current, *not* by the voltage value on the output pin. Therefore, there is no "C x V x F" dependency on the external dynamic current

of the Link Ports. Also, external capacitive loading on the LVDS drivers has no effect on the current consumed by the Link Ports.

A portion of the internal static current is due to the active circuitry of the Link Port and its related logic; this component is independent of the data width of the Link Port (1-bit or 4-bit mode).
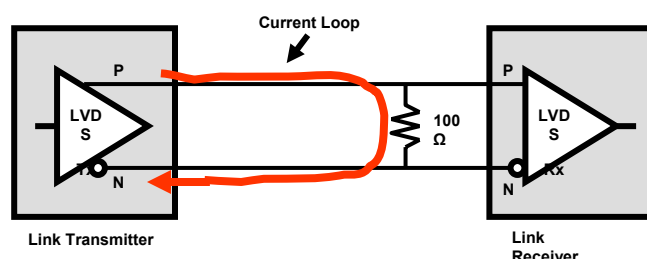


Figure 3. LVDS Current Loop Through Terminating Resistor

The remainder of the internal static current of the Link Port is determined by the termination scheme on the differential pin pairs. Because the LVDS Link Ports utilize current-mode drivers, there is a contribution to the internal static current due to the current loop that connects the "P" and "N" differential-mode drivers via the 100 Ω terminating resistor across the "P" and "N" pins of the LVDS receiver. Figure 3 shows a graphical depiction of this current loop.

> The Link Ports on revision 1.2 (and newer) silicon have a 100 Ω terminating resistor incorporated on-chip across the Link Port receive LVDS P/N clock and data pin pairs. Therefore, the external 100 Ω terminating resistor (as shown in Figure 3) is not required on the PCB for designs using silicon revisions 1.2 and newer.

The internal dynamic current depends on the switching frequency of the output driver circuits and the capacitance of the related internal circuits. (Keep in mind that the majority of the dynamic switching is due to the differential data and clock pairs of the Link Port; although the single-ended block completion output and acknowledge signals are active during Link Port

activity, their contributions to the overall switching can be ignored.)

Table 4 shows the total current value per Link Port for different frequencies, data widths, data activity levels, and termination schemes. (The unused LVDS data pin-pairs for 1-bit mode in this table were left unconnected, as described in the following paragraphs.) The values shown were taken at $T_{CASE}$ = 85°C and $V_{DD\_IO}$ = 2.5 V.

| | 1-bit | 1-bit | 4-bit | 4-bit |
|---|---|---|---|---|
| freq (MHz) | typ (mA) | max (mA) | typ (mA) | max (mA) |
| no connect | 13.25 | 13.25 | 13.25 | 13.25 |
| 0 | 20.50 | 20.50 | 31.00 | 31.00 |
| 125 | 33.75 | 35.00 | 34.25 | 36.00 |
| 250 | 36.25 | 40.00 | 37.25 | 41.00 |
| 333 | 37.75 | 43.50 | 39.25 | 44.25 |
| 500 | 41.75 | 50.50 | 43.75 | 50.50 |

Table 4. Link Port Current Consumption per Link Port

The first column lists the different Link Port operating frequencies. The "*no connect*" entry refers to a transmitting Link Port that is not connected to an LVDS receiver. In this case, there is no current loop present to contribute to the internal static current because there is an open circuit on the differential pair. The "*0 MHz*" entry refers to a Link Port that *is* connected to an LVDS receiver, but it is not active or enabled. The other entries in this column refer to the respective frequencies of the active Link Port. The "*typ*" and "*max*" columns refer to the switching activity on the LVDS outputs. The "*typ*" label refers to 50% of the data pins switching per link clock edge; the "*max*" label refers to 100% of the data pins switching per link clock edge. (Note that the Link Ports drive and receive data on each edge of the link clock.)

## Link Port 1-Bit Mode Termination Schemes

For 1-bit operating mode, Analog Devices, Inc. recommends the following termination scheme to ensure the minimal amount of current consumed by each transmitting Link Port. Terminate the active LVDS data pin pair with the 100 Ω resistor across the P/N receive pin pair, but leave

the remaining three unused transmitting LVDS data pin pairs unconnected. This will result in the lowest-possible current consumption by the Link Port, and will also save board space and reduce the number of components in the bill of materials (BOM) for the system board, since no signals need to be brought out from the processor package.

Assume that a processor in the example system has two active Link Ports (both receive and transmit channels active per Link Port), one in 1-bit mode and the other in 4-bit mode running at 250 MHz, with both switching at a "typical" data rate. (Note that the external dynamic power consumed by the Link Port is due to the transmitting link only.) Also assume that one of the remaining two inactive Link Ports is connected to an LVDS receiver, and the other is left unconnected.

*Link Port 0: unconnected*
*Link Port 1: connected/1-bit mode/0 MHz*
*Link Port 2: 1-bit mode/250 MHz/typical switching*
*Link Port 3: 4-bit mode/250 MHz/typical switching*

*Example 11. Link Port Configuration*

The total current consumed by the Link Ports ($I_{DD\_IO\_LP}$) for this example system can be calculated as shown in Example 12:

$$\begin{aligned} I_{DD\_IO\_LP} &= L.P.0 + L.P.1 + L.P.2 + L.P.3 \\ &= 13.25 + 20.50 + 36.25 + 37.25 \\ &= 107.25 \ mA \end{aligned}$$

*Example 72. Total Link Port Current Estimation*

### Total Estimated I/O Current ($I_{DD\_IO}$)

The total current $I_{DD\_IO}$ consumed on the $V_{DD\_IO}$ domain can be calculated by the sum of the total estimated External Port and Link Port current:

$$I_{DD\_IO} = I_{DD\_IO\_LP} + I_{DD\_IO\_EP}$$

*Equation 15. Total Estimated I/O Current*

Therefore, for the example system with two active Link Ports per processor, and the above

mentioned activity on the Cluster Bus, for each processor in the system, $I_{DD\_IO}$ can be calculated as follows:

$$\begin{aligned} I_{DD\_IO} &= I_{DD\_IO\_LP} + I_{DD\_IO\_EP} \\ &= 107.25 \ mA + 18.1 \ mA \\ &= 125.35 \ mA \end{aligned}$$

*Example 13. Total Estimated I/O Current*

### Total Estimated I/O Power ($P_{DD\_IO}$)

The total power ($P_{DD\_IO}$) consumed on the $V_{DD\_IO}$ domain for each processor can be calculated by multiplying the total estimated I/O current $I_{DD\_IO}$ by $V_{DD\_IO}$:

$$P_{DD\_IO} = V_{DD\_IO} * I_{DD\_IO}$$

*Equation 16. Total Estimated I/O Power*

Therefore, for the example system $P_{DD\_IO}$ can be calculated for each processor, as follows:

$$\begin{aligned} P_{DD\_IO} &= V_{DD\_IO} * I_{DD\_IO} \\ &= 2.5 \ V * 125.35 \ mA \\ &= 313.4 \ mW \end{aligned}$$

*Example 14. Total Estimated I/O Power*

## Power Supply Design

The previous three sections have shown how to estimate the average current consumption values on the $V_{DD}$, $V_{DD\_DRAM}$, and $V_{DD\_IO}$ voltage domains for a given system. This section describes the parameters used when designing the power supply for the TigerSHARC® system.

The power supply must be capable of handling worst-case sustainable power consumption for extended periods of time for each of the processor's three voltage domains.

Use the "Maximum Baseline Static Current" and "Baseline Dynamic Current" curves to calculate the maximum $I_{DD}$ current consumption that the power supply system design must be able to provide for the processor core. Additionally, use guard-banded values for the external I/O current

and worst-case internal DRAM current requirements ($I_{DD\_IO}$, and $I_{DD\_DRAM}$, respectively), as well as the maximum specified voltages for $V_{DD}$, $V_{DD\_IO}$, and $V_{DD\_DRAM}$.

Using these values ensures that the power supply design will provide maximum sustainable power at its highest efficiency (typically greater than 90%), to all of the voltage domains during sustained periods of maximum activity.

> (i) The data in the two "Maximum Baseline Static Current" curves in Appendix A refer to ADSP-TS201S devices shipped before and after October 2005 (date code 0549).

The "Maximum Baseline Static Current" curves show the maximum static current consumed by an individual ADSP-TS201S device for a given fabrication process. This differs from the "Typical Static Baseline Current" graph, which represents the statistical average value for all ADSP-TS201S processors, and is independent of fabrication process.

For the $V_{DD}$ voltage domain, the power supply design must be capable of supplying the maximum sustainable power consumption under the worst-case operating conditions. The "Maximum Baseline Static" and "Baseline Dynamic" characteristic curves can be used to find the worst-case current for $I_{DD}$. For our example, assume the following worst-case system conditions apply:

- $V_{DD}$ = maximum system value (1.05 V + 5%)
- $f$ = 500 MHz
- $T_{CASE}$ = maximum system value (55°C)

Multiply this value by the highest activity factor that is used in the system to achieve the value for the worst-case sustainable current draw on the core supply of the processor on the $V_{DD}$ domain.

Assume the above parameters for the following example calculation:

**Step 1:**
$$I_{DD\_DYN} = I_{DD\_BASELINE} \text{ x } I_{DD\_COMP\_HIGH} \text{ } Activity \text{ } Factor$$
$$= 2.15 \text{ A x } 1.0$$
$$= 2.15 \text{ A}$$

**Step 2:**
$$I_{DD} = I_{DD\_DYN} + I_{DD\_STATIC}$$
$$= 2.15 \text{ A} + 0.52 \text{ A}$$
$$= 2.67 \text{ A}$$

**Step 3:**
$$P_{DD} (max) = V_{DD} \text{ x } (I_{DD} + I_{DD\_A(max)})$$
$$= 1.10 \text{ V x ( } 2.67 \text{ A} + 0.05 \text{ A})$$
$$= 2.99 \text{ W}$$

*Example 15. $V_{DD}$ Power Supply*

Therefore, from this example, the power supply must be capable of providing 2.99 W on the $V_{DD}$ supply under sustained periods of activity at high efficiency for each processor in the system.

For the $V_{DD\_IO}$ voltage domain, the power supply design for this example must be capable of supplying a guard-banded conservative power consumption estimate for I/O activity ($V_{DD\_IO}$ = 2.63 V). This ensures sufficient overhead in the power supply design during sustained periods of high activity on the I/O domain.

$$P_{DD\_IO} (max) = I_{DD\_IO} * V_{DD\_IO} (max)$$

*Equation 17. $V_{DD\_IO}$ Power Supply Example*

For the $V_{DD\_DRAM}$ voltage domain, the power supply design must be capable of handling an estimated maximum value of *600 mW* for this domain ($P_{DD\_DRAM}$) for sustained periods of activity.

$$P_{DD\_DRAM} (max) = I_{DD\_DRAM} (max) * V_{DD\_DRAM} (max)$$
$$= 600 \text{ mW}$$

*Example 16. $V_{DD\_IO}$ Power Supply*

## Thermal Relief Design

The overall system power estimation can also be used to estimate a thermal relief budget. Equation gives a value for the total maximum estimated thermal power for a single ADSP-TS201S device in a given system.

Using maximum values in this equation is recommended for a thermal relief design that will allows the system to operate within specified thermal parameters under all operating conditions, since using these maximum values provides sufficient headroom (i.e., guard-band) in the thermal relief system design.

$$P_{TOTAL} = P_{DD} \ (max) + P_{DD\_IO} \ (max) + P_{DD\_DRAM} \ (max)$$

*Equation 18. Total Estimated Thermal Power*

# Appendix A

Appendix A contains three different baseline static curves. Each curve represents different values for $I_{DD\_STATIC}$, which apply to different ADSP-TS201S processor date codes. The date codes provided in this section are preliminary. Contact Analog Devices for more information.
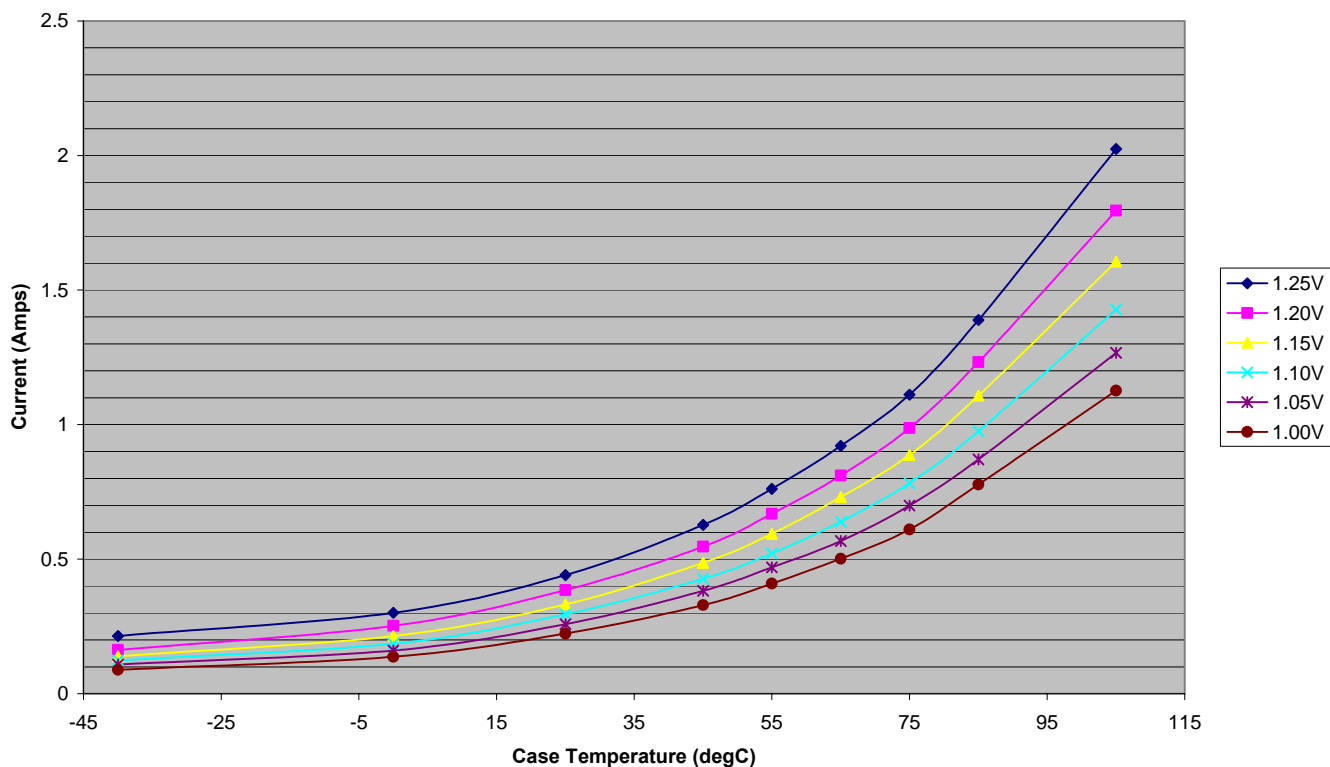
## Typical Baseline Static Current

**ADSP-TS201S - Typical Baseline Static Idd Current vs. Case Temperature**
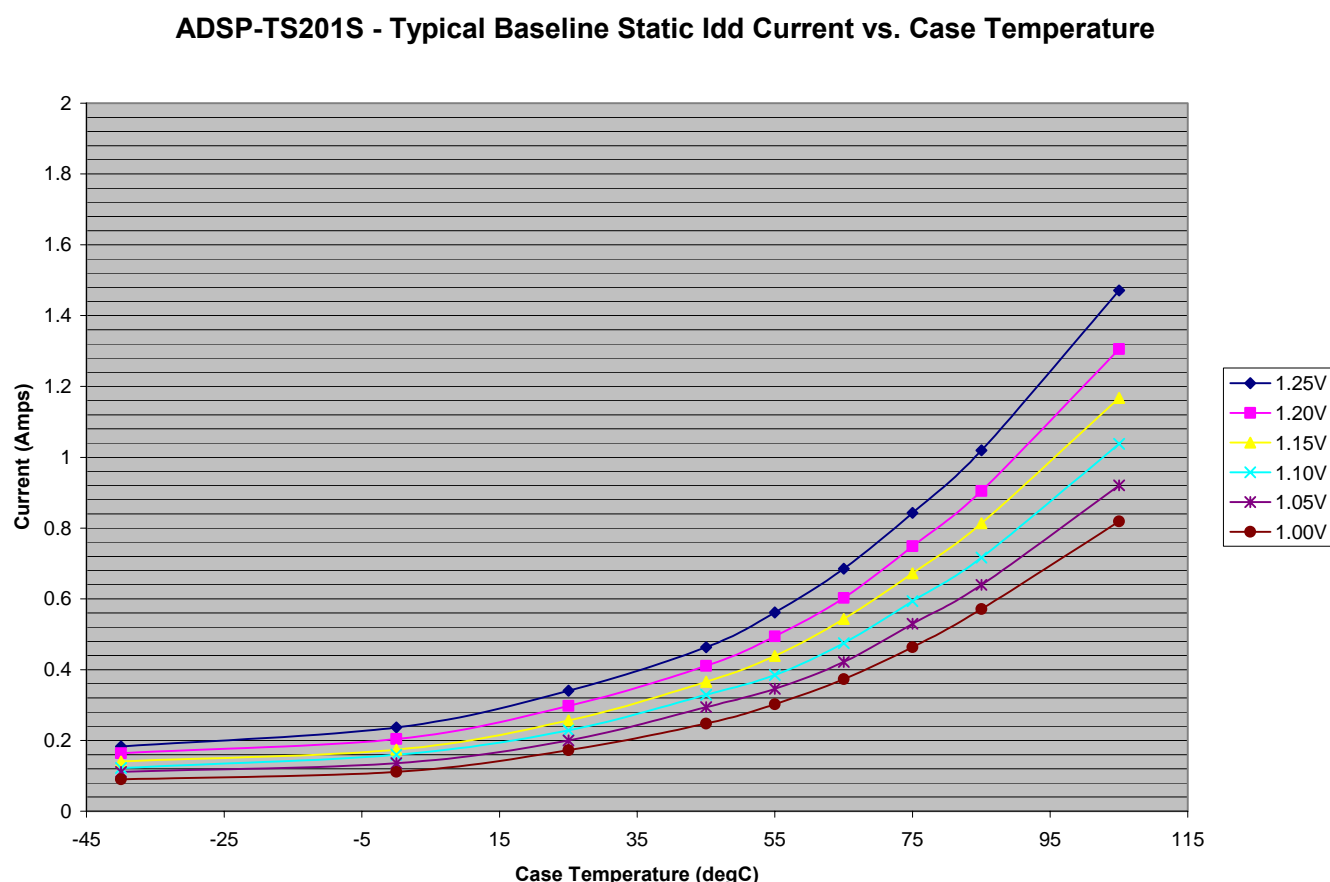


The "Typical Baseline Static Current" graph also appears in Figure 2 on page 5 of this document. Consider the curves in this graph when calculating the average static power consumed by each processor in a system. The data represented in this figure applies to all date codes, since this data represents the statistical average static current for all ADSP-TS201S processors.

## Maximum Baseline Static Current (Date Code 0549 or newer)

**ADSP-TS201S - Maximum Baseline Static Idd Current vs. Case Temperature**
**(For Date Codes 0549 Or Newer)**



Use the curves in this "Maximum Baseline Static Current" graph to calculate the maximum static power consumed by each processor in a system. The data in this figure is worst-case data and applies to specific ADSP-TS201S devices shipped on or after October 2005 (date code 0549). For more information on the appropriate date code, contact Analog Devices.

**Maximum Baseline Static Current (Date Code 0549 or older)**

### ADSP-TS201S: Idd Baseline Static Current vs. Case Temperature (For Current Devices and Date Codes Up To 0549)
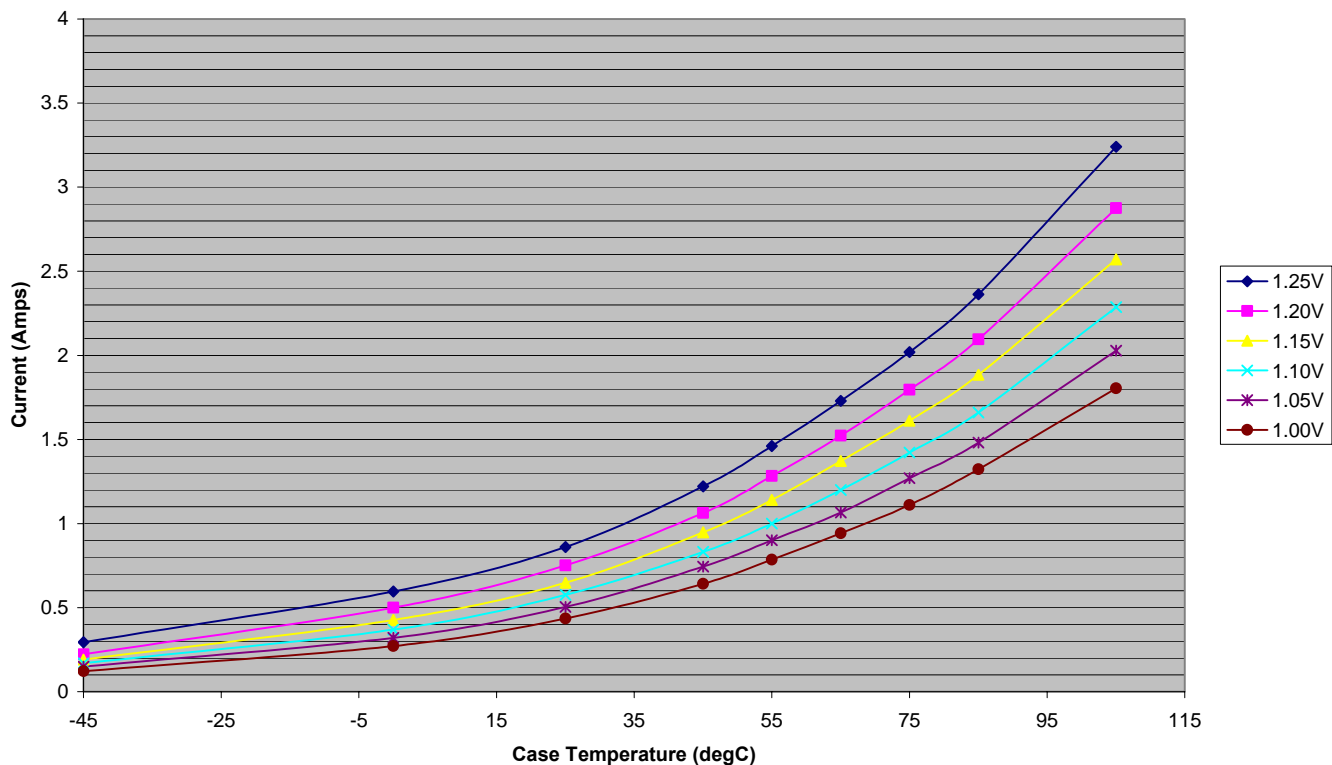


Use the curves in this figure to calculate the maximum static power consumed by each processor in a system. The data in this figure is worst-case data and applies to specific ADSP-TS201S devices shipped before October 2005 (date code 0549 or older). For more information on the appropriate date code, contact Analog Devices.

# Appendix B

Appendix B contains the Maximum Baseline Dynamic Current graph, which represents values for $I_{DD\_DYN}$. This graph appears in Figure 1 on page 3 of this document. The information in this graph pertains to all date codes and revisions of ADSP-TS201S processors.

**ADSP-TS201S Dynamic IDD Compute High Activity**
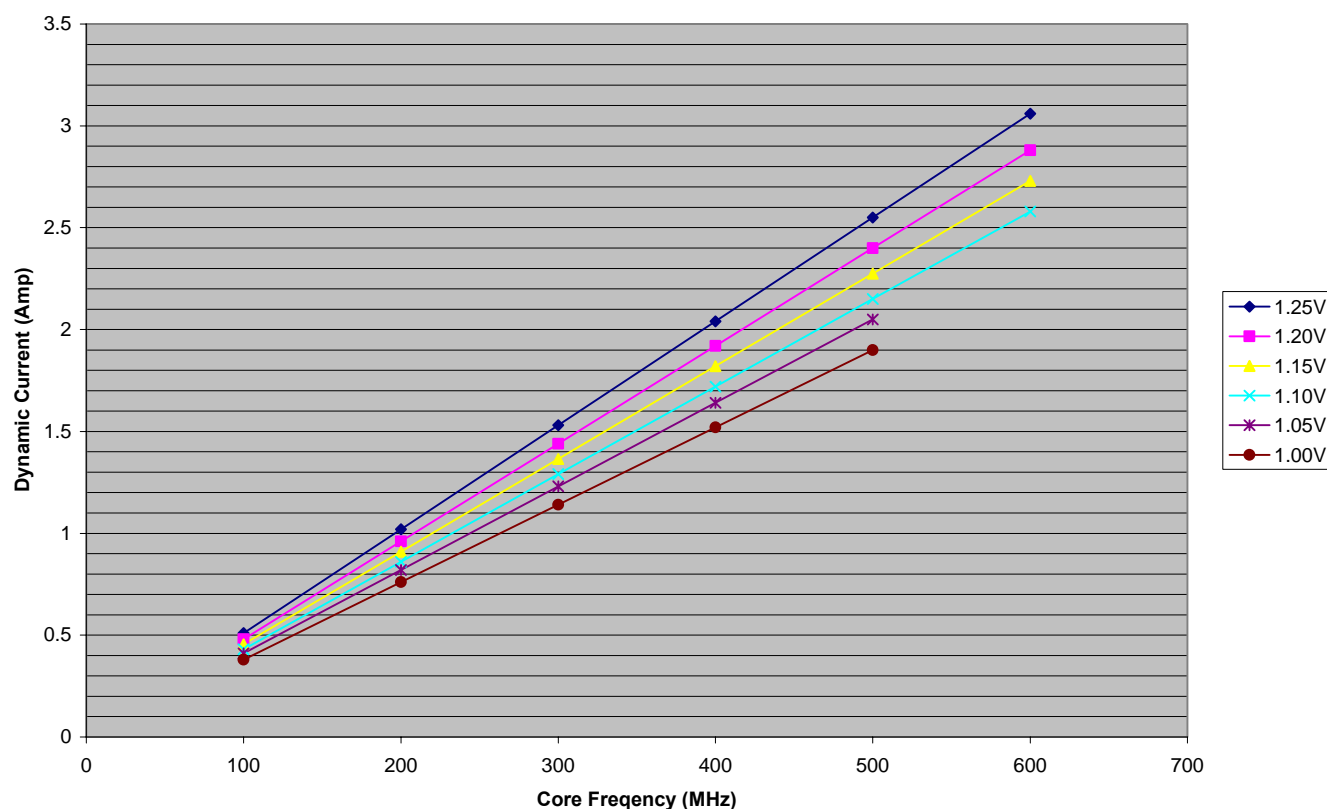


# Document History

| Revision | Description |
|---|---|
| *Rev 1 –January 03, 2005 by Greg F.* | Initial Public Release |